WHAT IS CLAIMED IS:

1. A timing adjustment circuit which is fed with an input positive-logic signal that is asserted at its high level, and an input negative-logic signal that is asserted at its low level, and which generates an output positive-logic signal and an output negative-logic signal that have their phase difference decreased, characterized by comprising:

a signal generation portion which generates a reference signal on the basis of either of the input positive-logic signal and the input negative-logic signal, and which generates a signal to-be-corrected on the basis of the other signal; and

a correction portion which corrects the signal to-be-corrected on the basis of the reference signal;

wherein said reference signal is delivered as one of the output positive-logic signal and the output negative-logic signal, while a signal obtained by correcting said signal to-be-corrected by means of the first correction circuit and the second correction circuit is delivered as the other of said output positive-logic signal and said output negative-logic signal.

2. A timing adjustment circuit characterized in that said correction portion includes:

a first correction portion which corrects a timing of a trailing edge of said signal to-be-corrected on the basis of a leading edge of said reference signal; and

a second correction portion which corrects a timing of a leading edge of said signal to-be-corrected on the basis of a trailing edge of said reference signal.

3. The timing adjustment circuit as defined in claim 2, characterized in that either of said first correction portion and said second correction portion is a NAND circuit, while the other is a NOR circuit.

4. The timing adjustment circuit as defined in claim 3, characterized by comprising:

a first wiring line which is fed with said reference signal; and

a second wiring line which is fed with said signal to-be-corrected;

wherein one input terminal of said NAND circuit is connected to said first wiring line, while the other input terminal thereof is connected to said second wiring line, and an output terminal of said NAND circuit is connected to said second wiring line; and

one input terminal of said NOR circuit is connected to said first wiring line, while the other input terminal thereof is connected to said second wiring line, and an output terminal of said NOR circuit is connected to said second wiring line.

5. The timing adjustment circuit as defined in claim 2, characterized in that said reference signal advances in phase relative to said signal to-be-corrected.

6. The timing adjustment circuit as defined in claim 5, characterized in:

that said reference signal is asserted at its high level, while said signal to-be-corrected is asserted at its low level;

wherein said first correction circuit is said NAND circuit; and

said second correction circuit is said NOR circuit.

7. The timing adjustment circuit as defined in claim 5, characterized in:

that said reference signal is asserted at its low level, while said signal to-be-corrected is asserted at its high level;

wherein said first correction circuit is said NOR circuit; and

said second correction circuit is said NAND circuit.

8. The timing adjustment circuit as defined in claim 2, characterized in that said reference signal retards in phase relative to said signal to-be-corrected.

9. The timing adjustment circuit as defined in claim 8, characterized in:

that said reference signal is asserted at its high level, while said signal to-be-corrected is asserted at its low level;

wherein said first correction circuit is said NOR circuit; and

said second correction circuit is said NAND circuit.

10. The timing adjustment circuit as defined in claim 8, characterized in:

that said reference signal is asserted at its low level, while said signal to-be-corrected is asserted at its high level;

wherein said first correction circuit is said NAND circuit; and

said second correction circuit is said NOR circuit.

11. The timing adjustment circuit as defined in claim 1, characterized in that said signal generation portion includes a first inversion circuit which inverts either of said input positive-logic signal and said input negative-logic signal, thereby to generate said reference signal, and a second inversion circuit which inverts the other signal, thereby to generate said signal to-be-corrected.

12. The timing adjustment circuit as defined in claim 1, characterized in:

that a single input signal is fed to said signal generation portion instead of said input positive-logic signal and said input negative-logic signal;

wherein said signal generation portion generates said reference signal and said signal to-be-corrected on the basis of the input signal.

13. The timing adjustment circuit as defined in claim 12, characterized in that said signal generation portion includes:

a first inversion circuit which inverts said input signal at least once, thereby to generate said reference signal; and

a second inversion circuit which inverts said input signal more than the number of times of inversion of said first inversion circuit, thereby to generate said signal to-be-corrected.

14. A drive circuit which drives an electrooptic device having a plurality of scanning lines, a plurality of data lines, and pixel electrodes and switching elements that are arranged in the shape of a matrix in correspondence with intersections between the scanning lines and the data lines, characterized by comprising:

the timing adjustment circuit as defined in claim 1, wherein the timing of a predetermined signal is adjusted using said timing adjustment circuit.

15. An electrooptic device comprising:

a plurality of scanning lines;

a plurality of data lines;

pixel electrodes and switching elements which are arranged in the shape of a matrix in correspondence with intersections between said scanning lines and said data lines; and

the drive circuit as defined in claim 14.

16. An electronic equipment characterized by comprising the electrooptic device as defined in claim 15.